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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,204	ODA, NORIAKI	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14 and 42-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 14 and 42-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/761204 Attorney's Docket #: 8017-1122
Filing Date: 1/22/2004; claimed foreign priority to 1/30/2003

Applicant: Oda Examiner: Alexander Williams

Applicant's Amendment filed 2/16/07 to the election of the species of figure 2 (claims 1 to 11, 14 and 42 to 49), filed 8/30/05, has been acknowledged.

Claims 2, 12, 13 and 15 to 41 have been cancelled.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the upper copper layer is separated from the lower surface of said bonding pad only by the barrier metal in claims 50 and 51 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 50 and 51 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 50 and 51, it is unclear and confusing to what is meant by and what shows "wherein the upper copper layer is separated from the lower surface of said bonding pad only by the barrier metal." In Applicant's figure 2A, the barrier metal is 54, the upper copper layer 120, the lower surface of the bonding pad 130 is separate except for when the bonding pad is bend upwards and a portion of layer 52 is between the corner of the upper copper layer and the lower surface of the bonding pad end portion. Therefore, Applicant's statement does not appear to be correct language.

Any of claims 50 and 51 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 to 11 and 14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Watanabe (U.S. Patent Application Publication # 2003/0047794 A1).

1. Watanabe (figures 1 to 13) specifically figure 1 show a semiconductor device, comprising: a bonding pad **50** on a semiconductor substrate **1**; an upper copper layer **27** on a lower surface of said bonding pads with a barrier metal **51** interposed; and a lower copper layer **25** closer to said semiconductor substrate than said upper copper layer; wherein a copper area ratio of said lower copper layer under said bonding pad is lower than that of said upper copper layer, and wherein said lower copper layer is not electrically connected to said upper copper layer under said bonding pad.

[0051] For example, the pad 50 is made of AlCu alloy (Cu content: 0.5 wt %) and has a thickness of 1000 nm, and each of the barrier metal layers 51 and 52 is made of TiN and has a thickness of 50 nm. A conductive wire 75 is wire-bonded to the upper surface of the pad 50. The conductive wire 75 is electrically connected to a semiconductor device formed on the surface of the semiconductor substrate 1, e.g., MOSFET 6, via the pads 27 and plugs 36 of the underlying wiring layers.

3. A semiconductor device according to claim 1, Watanabe show wherein the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

4. A semiconductor device according to claim 1, Watanabe show wherein the copper area ratio of said upper copper layer is at least 70%.

5. A semiconductor device according to claim 1, Watanabe show wherein the planar dimensions of said bonding pads and said upper copper layer are substantially equal.

6. A semiconductor device according to claim 1, Watanabe show wherein said upper copper layer is constituted by a plurality of copper layers.

7. A semiconductor device according to claim 6, Watanabe show wherein the copper area ratios of each copper layer of said upper copper layer are substantially the same.

8. A semiconductor device according to claim 6, Watanabe further comprising: interlevel dielectric films that are provided between each of the copper layers of said upper copper layer; and via-plugs composed of copper that are embedded in said interlevel dielectric films wherein each of the copper layers of said upper copper layer are connected by way of said via-plugs.

9. A semiconductor device according to claim 8, Watanabe show wherein the copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and said via-plugs that are connected to the copper layer pattern are embedded in a dielectric film that is composed of a first material.

10. A semiconductor device according to claim 1, Watanabe show wherein the copper area ratio of said lower copper layer is at least 15% and not greater than 95%.

11. A semiconductor device according to claim 1, Watanabe show wherein said lower copper layer is constituted by a plurality of copper layers.

14. A semiconductor device according to claim 13, Watanabe show wherein each of the copper layers of said lower copper layer are constituted by a copper pattern that is embedded in a dielectric film that is composed of a second material having a lower relative dielectric constant than said first material.

Claims 1, 3 to 11 and 14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Hatano et al. (U.S. Patent Application Publication # 2002/0163083 A1).

1. Hatano et al. (figures 1 to 15B) specifically figure 1A show a semiconductor device, comprising: a bonding pad **112** on a semiconductor substrate **101**; an upper copper layer **108** on a lower surface of said bonding pads with a barrier metal **111** interposed; and a lower copper layer **104** closer to said semiconductor substrate than said upper copper layer; wherein a copper area ratio of said lower copper layer under said bonding pad is lower than that of said upper copper layer, and wherein

said lower copper layer is not electrically connected to said upper copper layer under said bonding pad.

[0041] At the same time, another contact via which reaches the copper pad 124 is formed on a portion of the silicon nitride film 109 and silicon oxide film 110 in the interconnect formation area B as shown in FIG. 1B. A titanium nitride layer 125, aluminum interconnect 126, and titanium nitride layer 127 are sequentially formed on the top surface side of the copper interconnect 124. The titanium nitride layer 125, aluminum interconnect 126, and titanium nitride layer 127 are electrically connected to the copper interconnect 124 through the contact via. The titanium nitride layer 125, aluminum interconnect 126, and titanium nitride layer 127 are formed by a process that is identical to the process for forming the titanium nitride layer 111, aluminum pad 112, and titanium nitride layer 113, at substantially the same time. The aluminum interconnect 126 is formed with the same material as that for the aluminum pad 112.

[0042] The silicon oxide film 110, titanium nitride layer 113, and titanium nitride layer 127 are covered with the insulator protection film 114. An aperture, which reaches the aluminum pad 112, is formed on the insulator protection film 114. A bonding wire not shown in the figure is connected to the aluminum pad 112 through the aperture.

[0043] FIGS. 2 through 10 illustrate an embodiment of a manufacturing method of a semiconductor device according to the present invention.

[0044] As shown in FIGS. 2A and 2B, a silicon oxide film 202 is formed on the top surface of a silicon substrate 201. A copper interconnect forming trench 231 is formed on the silicon oxide film 202 in both the bonding pad formation area A and interconnect formation area B.

[0045] Continuing, a barrier metal film is formed on the entire surface of the top surface side of the silicon substrate 201. The barrier metal film is formed by a conductive film capable of preventing copper diffusion. A copper film is formed on that barrier metal film through an electroplating method. In

addition, the portion of the formed barrier metal film and copper film other than the portion within the copper interconnect forming trench 231 is removed through a CMP method. As shown in FIG. 3A, the barrier metal film 203 and copper interconnect 204 are formed within the copper interconnect forming trench 231 in the bonding pad formation area A. Moreover, as shown in FIG. 3B, the barrier metal film 221 and copper interconnect 222 are formed within the copper interconnect forming trench 231 in the interconnect formation area B.

[0046] Continuing, as shown in FIGS. 4A and 4B, the copper diffusion preventive film 205 is formed on the silicon oxide film 202, barrier metal film 203, copper interconnect 204, barrier metal film 21, and copper interconnect 222. The copper diffusion preventive film 205 is formed with a material to prevent copper diffusion, such as a silicon nitride. Moreover, a silicon oxide film 206 is formed on the copper diffusion preventive film 205. Continuing, a copper pad forming trench 233 and a copper interconnect forming trench 234 are formed on the silicon oxide film 206, substantially at the same time. The copper pad forming trench 233 is formed within the bonding pad formation area A, whereas the copper interconnect forming trench 234 is formed within the interconnect formation area B. Moreover, a copper interconnect contact via 232a and a copper interconnect contact via 232b are formed from the respective bottom surfaces of the copper pad forming trench 233 and the copper interconnect forming trench 234, substantially at the same time. The copper interconnect contact via 232a reaches the copper interconnect 204 from the bottom surface of the copper pad forming trench 233. Similarly, the copper interconnect contact via 232b reaches the copper interconnect 222 from the bottom surface of the copper interconnect forming trench 234.

[0047] Continuing, a barrier metal film is formed at the entire surface at the top surface side of the silicon substrate 201. The barrier metal film is formed by a conductive film capable of preventing copper diffusion. A copper film is formed on the barrier metal film through an electroplating method. In addition, a portion other than the portions within the copper interconnect contact via 232a, copper interconnect contact via 232b, copper pad forming trench 233, and copper interconnect forming trench 234 of the formed barrier metal film and copper film is removed through a CMP method. As shown in FIG.

5A, a barrier metal film 207 and copper pad 208 are formed in the bonding pad formation area A so as to embed the copper interconnect contact via 232a and copper pad forming trench 233. As shown in FIG. 5B, a barrier metal film 223 and copper interconnect 224 are formed in the interconnect formation area B so as to embed the copper interconnect contact via 232b and copper interconnect forming trench 234.

3. A semiconductor device according to claim 1, Hatano et al. show wherein the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

4. A semiconductor device according to claim 1, Hatano et al. show wherein the copper area ratio of said upper copper layer is at least 70%.

5. A semiconductor device according to claim 1, Hatano et al. show wherein the planar dimensions of said bonding pads and said upper copper layer are substantially equal.

6. A semiconductor device according to claim 1, Hatano et al. show wherein said upper copper layer is constituted by a plurality of copper layers.

7. A semiconductor device according to claim 6, Hatano et al. show wherein the copper area ratios of each copper layer of said upper copper layer are substantially the same.

8. A semiconductor device according to claim 6, Hatano et al. further comprising: interlevel dielectric films that are provided between each of the copper layers of said upper copper layer; and via-plugs composed of copper that are embedded in said interlevel dielectric films wherein each of the copper

layers of said upper copper layer are connected by way of said via-plugs.

9. A semiconductor device according to claim 8, Hatano et al. show wherein the copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and said via-plugs that are connected to the copper layer pattern are embedded in a dielectric film that is composed of a first material.

10. A semiconductor device according to claim 1, Hatano et al. show wherein the copper area ratio of said lower copper layer is at least 15% and not greater than 95%.

11. A semiconductor device according to claim 1, Hatano et al. show wherein said lower copper layer is constituted by a plurality of copper layers.

14. A semiconductor device according to claim 13, Hatano et al. show wherein each of the copper layers of said lower copper layer are constituted by a copper pattern that is embedded in a dielectric film that is composed of a second material having a lower relative dielectric constant than said first material.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a plurality of copper layers and a copper layer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an

article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 42-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (U.S. Patent Application Publication # 2003/0047794 A1).

42. Watanbe (figures 1 to 13) specifically figure 1 show a semiconductor device comprising: a bonding region in which a bonding pad **50** is formed; an internal circuit region provided inside of said bonding region, said internal circuit region having a multilevel' wiring structure that includes a plurality of copper interconnect layers at **27** a first level and a plurality of copper interconnect layers **25** at second level; and

an upper copper layer **(27 under 50)** formed in said bonding region above said internal circuit region and under said bonding pad in electrical contact therewith, one of said copper interconnect layers at said first level being elongated from

said internal circuit region to said bonding region under said upper copper layer in electrical isolation therefrom.

43. The device as claimed in claim 42, Watanabe show wherein one of said copper interconnect layers at said second level is further elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation from said copper layer and from one of said copper interconnect layers at said first level.

44. The device as claimed in claim 42, Watanabe show wherein said upper copper layer includes first and second copper layers and a via-plug sandwiched therebetween.

45. The device as claimed in claim 44, Watanabe show further comprises a plurality of copper interconnect layers at a third level and a plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

46. The device as claimed in claim 45, Watanabe show wherein said bonding pad is in electrical contact with said second copper layer, and one of said copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

47. The device as claimed in claim 43, Watanabe show wherein said upper copper layer includes first and second copper layers and a via plug sandwiched therebetween, and said bonding pad is in electrical contact with said second copper layer.

48. The device as claimed in claim 47, Watanabe further comprising a plurality of copper interconnect layers at a third level and a plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.
49. The device as claim in claim 48, Watanabe show wherein said bonding pad is in electrical contact with said second copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

Therefore, it would have been obvious to one of ordinary skill in the art to use the copper layer and the plurality of copper layers as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 42-51, insofar as claims 50 and 51 can be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al. (U.S. Patent Application Publication # 2002/0163083 A1).

42. Hatano et al. (figures 1 to 15B) specifically figure 1A show a semiconductor device comprising: a bonding region in which a bonding pad **112** is formed; an internal circuit region provided inside of said bonding region, said internal circuit region having a multilevel wiring structure that includes a plurality of copper interconnect layers at **108** a first level and a plurality of copper interconnect layers **104** at second level; and

an upper copper layer **(108 under 112)** formed in said bonding region above said internal circuit region and under said bonding pad in electrical contact therewith, one of said copper interconnect layers at said first level being elongated from said internal circuit region to said bonding region under said upper copper layer in electrical isolation therefrom.

43. The device as claimed in claim 42, **Hatano** et al. show wherein one of said copper interconnect layers at said second level is further elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation from said copper layer and from one of said copper interconnect layers at said first level.

44. The device as claimed in claim 42, **Hatano** et al. show wherein said upper copper layer includes first and second copper layers and a via-plug sandwiched therebetween.

45. The device as claimed in claim 44, **Hatano** et al. show further comprises a plurality of copper interconnect layers at a third level and a plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

46. The device as claimed in claim 45, **Hatano** et al. show wherein said bonding pad is in electrical contact with said second copper layer, and one of said copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

47. The device as claimed in claim 43, **Hatano** show wherein said upper copper layer includes first and second copper layers and a via plug sandwiched therebetween, and said bonding pad is in electrical contact with said second copper layer.

48. The device as claimed in claim 47, **Hatano** further comprising a plurality of copper interconnect layers at a third level and a

plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

49. The device as claim in claim 48, Hatano show wherein said bonding pad is in electrical contact with said second copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

50. The device as claim in claim 1, Hatano show the upper copper layer is separated from the lower surface of said bonding pad only by the barrier metal.

51. The device as claim in claim 42, Hatano show the upper copper layer is separated from the lower surface of said bonding pad only by the barrier metal.

Therefore, it would have been obvious to one of ordinary skill in the art to use the copper layer and the plurality of copper layers as "merely a matter of obvious engineering choice" as set forth in the above case law.

Response

Applicant's arguments filed 2/16/07 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at time.

Field of Search	Date
U.S. Class and subclass: 257/700,701,758,459,784,774,680,756,750,734,751,760,762,E23.02,E23.145,E21.582,E21.576	9/30/05 4/5/06 10/11/06 5/13/07
Other Documentation: foreign patents and literature in 257//700,701,758,459,784,774,680,756,750,734,751,760,762,E23.02,E23.145,E21.582,E21.576	9/30/05 4/5/06 10/11/06 5/13/07

Electronic data base(s): U.S. Patents EAST	9/30/05 4/5/06 10/11/06 5/13/07

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
5/13/07